## We claim:

- 1. An arrangement for protecting a high-frequency integrated circuit against higher voltages than normal operating voltages on an input/output terminal connected to a bonding pad, wherein the arrangement comprises a semiconductor varistor that is integrated between the bonding pad and the input/output terminal together with the integrated circuit and that has a low resistance for said normal operating voltages and a higher resistance for said higher voltages.
- 2. The arrangement according to claim 1, wherein the resistance for said normal operating voltages is essentially constant.
- 3. The arrangement according to claim 1, wherein an interconnection point between the varistor and the bonding pad is connected to a primary current shunting device.
- 4. The arrangement according to claim 3, wherein the primary current shunting device comprises a diode that is connected with its anode to the interconnection point between the varistor and the bonding pad and with its cathode to a positive voltage, and a diode that is connected with its cathode to the interconnection point between the varistor and the bonding pad and with its anode to ground.
- 5. The arrangement according to claim 1, wherein the interconnection point between the varistor and the integrated circuit is connected to a secondary current shunting device.
- 6. The arrangement according to claim 5, wherein the secondary current shunting device comprises a diode that is connected with its anode to the interconnection point between the varistor and the integrated circuit and with its cathode to a positive voltage, and a diode that is connected with its cathode to the interconnection point between the varistor and the integrated circuit and with its anode to ground.

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- 7. A protection arrangement comprising:
- a high-frequency integrated circuit comprising an input/output terminal and a bonding pad,
- a semiconductor varistor integrated between the bonding pad and the input/output terminal together with the integrated circuit which has a low resistance for a normal operating voltages and a higher resistance for higher voltages.
- 8. The arrangement according to claim 7, wherein the resistance for said normal operating voltages is essentially constant.
- 9. The arrangement according to claim 7, wherein an interconnection point between the varistor and the bonding pad is connected to a primary current shunting device.
- 10. The arrangement according to claim 9, wherein the primary current shunting device comprises a diode that is connected with its anode to the interconnection point between the varistor and the bonding pad and with its cathode to a positive voltage, and a diode that is connected with its cathode to the interconnection point between the varistor and the bonding pad and with its anode to ground.
- 11. The arrangement according to claim 9, wherein the interconnection point between the varistor and the integrated circuit is connected to a secondary current shunting device.
- 12. The arrangement according to claim 11, wherein the secondary current shunting device comprises a diode that is connected with its anode to the interconnection point between the varistor and the integrated circuit and with its cathode to a positive voltage, and a diode that is connected with its cathode to the interconnection point between the varistor and the integrated circuit and with its anode to ground.

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